**Face-To-Face Student/Supervisor Meeting Record**

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| **Project Title:** | Design and Implementation of a Multi-core Processor using FPGA | **Photo:** |  |
| **Student Name:** | Matteo Bovino | **Student ID:** | 8671055 |
| **Supervisor:** | Dr Server Kasap | **Student UID:** |  |
| **Supervisor UID:** |  | **Department:** | AAEEE |
| **Course Code:** | Electrical and Electronic Engineering | **Module Code:** | 306AAE |
| **Date Today:** | 05/03/2021 | **Time:** | 02:00 PM |

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| **Current Progress and Issues:** | |
| *In this meeting we discussed about the current development of the project, the results that have been achieved in the simulation environment and the remaining steps of the project. We also talked about the options available at the moment, and whether or not to continue with the actual implementation. The supervisor informed me about the updated university guidelines regarding the final year project. Due to the substantial progress made in the Vivado simulation environment and the extension of the project deadline, I decided to continue with the hardware implementation and not settle with the simulation results.* | |
| **Agreed Key Action Points:** | |
| *Based on the decision mentioned above, the supervisor has advised me to research the topics of synthesis and implementation in an in-depth manner. Although I previously programmed and worked with the Nexys4 DDR board, all the projects were of much more modest scale. Thus, I’ll revise with greater attention the documentation indicated by the supervisor before attempting the actual synthesis and implementation. If successful, the in-circuit test phase of the project will be the next step. Once the board is programmed according to the initial specifications, the dissertation and presentation will be undertaken.* | |
| **Date and Time of next meeting:** | 02:00 PM 19/03/2021 |

*Signatures of those present:*

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| **Supervisor:** |  |
| **Student: Matteo Bovino** |  |